IDEC Chip Design Contest

A W-band Divide-by-Three Injection Locked Frequency Divider with Injection Current Boosting Utilizing Inductive Feedback in 65nm CMOS

Hyohyun Nam and Jung-Dong Park

Division of Electronics and Electrical Engineering, Dongguk University

Introduction

- PLL (Phased-Locked Loop)는 mm-wave transceiver에 필수/핵심 블록임
- W-band에서 동작하는 PLL은 modulus의 초단 frequency divider (FD)가 VCO의 동작주파수를 커버하도록 wide-band로 설계되어야함
- Injection-locked (IL) 기반의 FD는 높은 주파수에서 저전력을 소비하며 동작하는 장점이 있으나, locking range가 제한됨
- Current Mode Logic (CML) 기반의 FD는 wide bandwidth가 구현 가능 하지만 높은 전력소모를 요구함
- 본 연구에서는 W-band에서 저전력을 소비하며 wide locking range가 구현 가능한 ILFD 설계방법을 제안함

< ILFD 동작원리 >

입력 트랜지스터의 Injection 전압에 의해 변환된 Injection 전류 (I_{inj})는 3 차 harmonics 가 2 차 harmonics와 Mixing 되어 입력 주파수의 1/3 주파수에 locking 됨 ILFD의 locking range는 I_{inj} 에 비례하며, I_{osc} (Mixer의 oscillation drain 전류)와 Q_R (Resonator의 quality factor)에 반비례함.

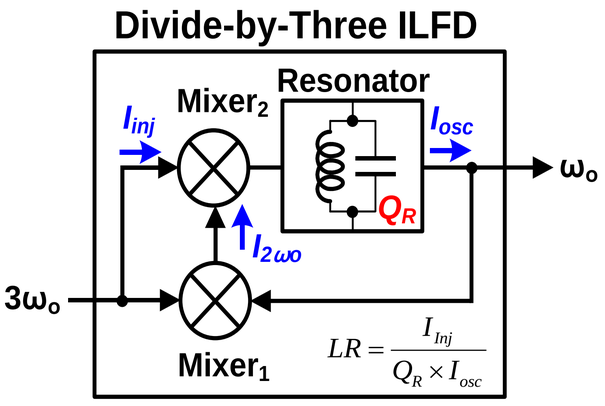

Fig. 1. A block diagram of the function of divide-by-three injection locked frequency divider (ILFD).

ILFD Design

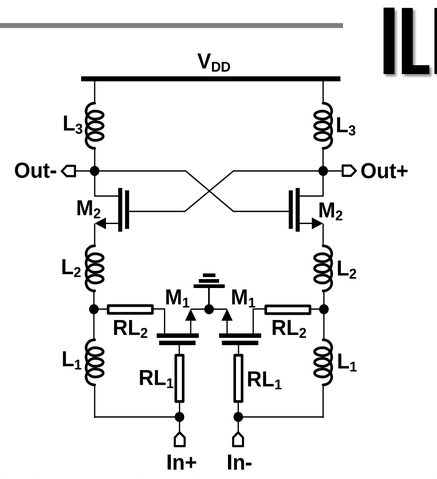

Fig. 2. Schematic of the proposed ILFD with inductive feedback for I_{inj} boosting.

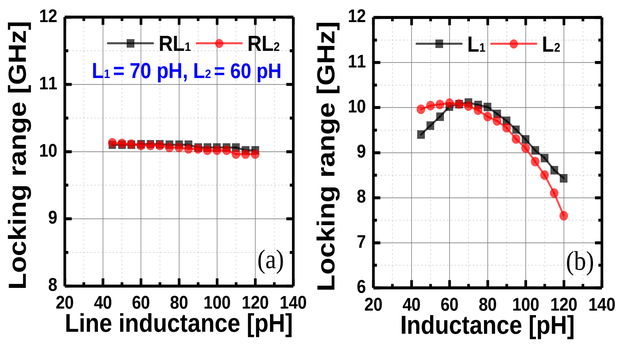

Fig. 3. (a) Locking range versus RL_1 and RL_2 with given L_1=70pH and L_2=60pH. (b) Locking range versus L_1 and L_2

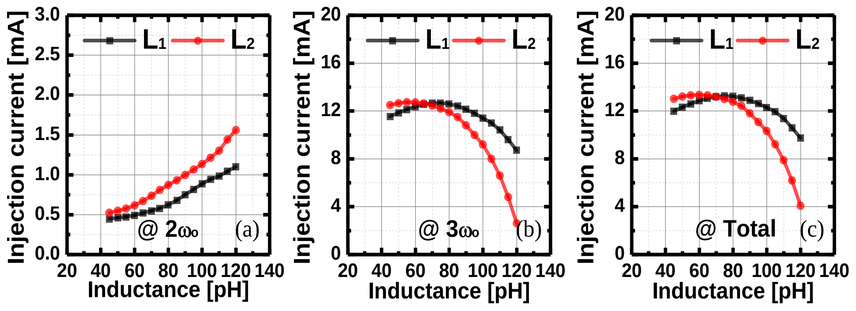

Fig. 4. Injection current at (a) $2\omega_o$, (b) $3\omega_o$, and (c) total ($I_{2\omega o}$+$I_{3\omega o}$) *versus* L_1 and L_2.

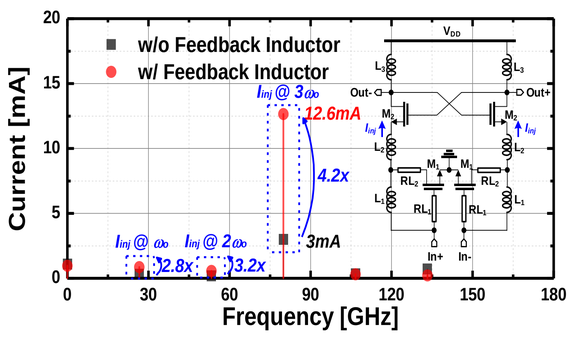

Fig. 5. Simulated injection current with and without feedback inductor for the proposed ILFD.

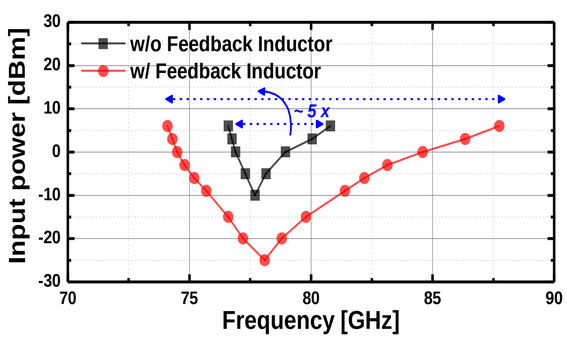

Fig. 6. Simulated locking range with and without feedback inductor for the proposed ILFD.

Measurement results

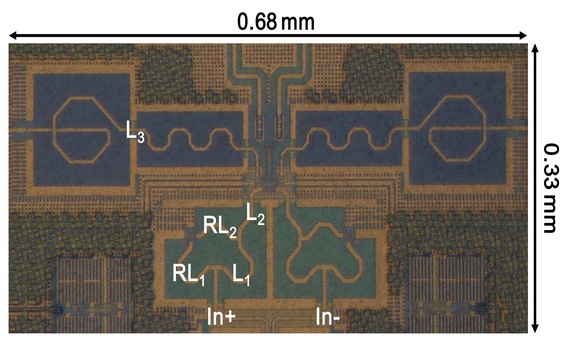

Fig. 7. A microphotograph of the proposed ILFD chip with the inductive feedback (core size: 0.68 x 0.33 mm^2).

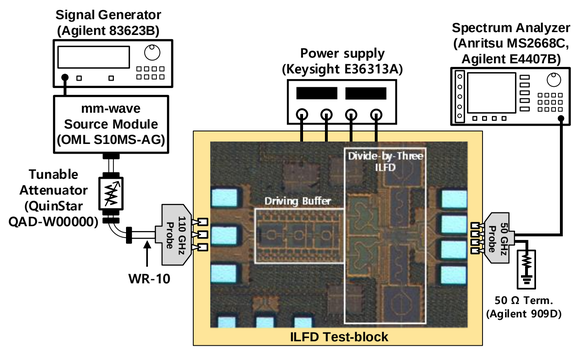

Fig. 8. Measurement set-up for the proposed ILFD test-block with driving buffer.

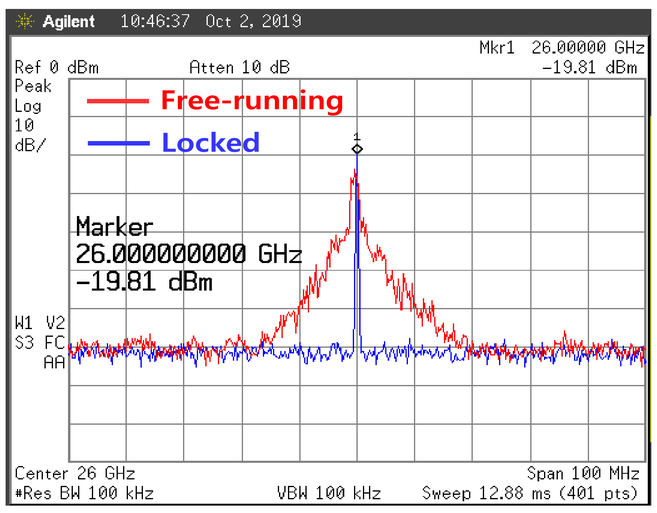

Fig. 9. Measured spectra in free-running and locking state for the proposed ILFD with input frequency of 78GHz.

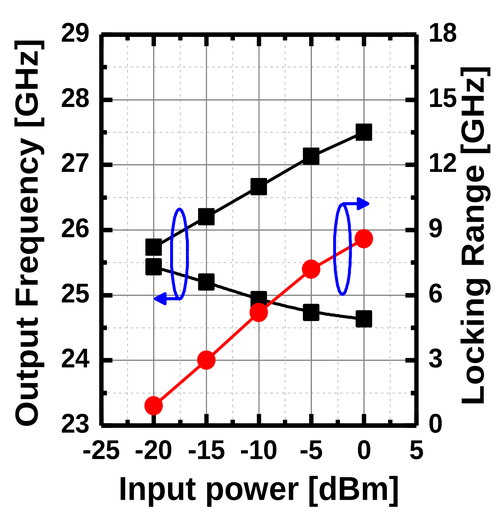

Fig. 10. Measured sensitivity curve and locking range for the proposed ILFD.

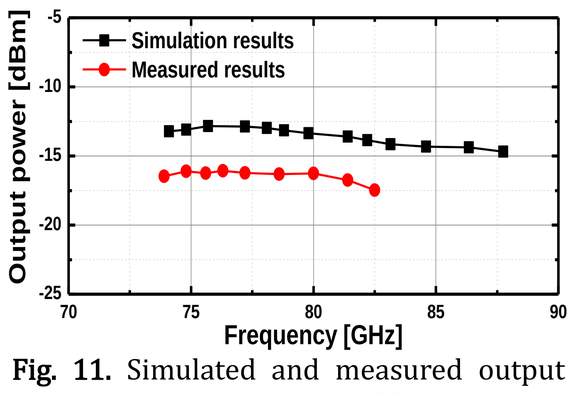

Fig. 11. Simulated and measured output power for the proposed ILFD with input power of 0dBm. The measured output power is considered the loss caused by probe-tip and cable.

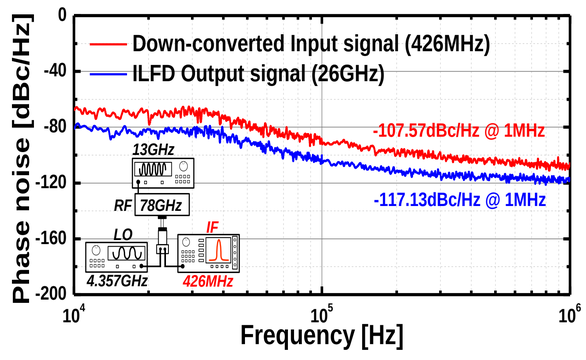

Fig. 12. Measured phase noise for the proposed ILFD in locking condition. The phase noise of the input frequency was measured using by harmonic mixer (Agilent 11970W).

Comparison table

Ref.	This work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Technology	**65nm CMOS**	**130nm CMOS**	**130nm CMOS**	**65nm CMOS**	**90nm CMOS**	**90nm CMOS**	**65nm CMOS**	**65nm CMOS**
Max. Frequency [GHz]	**82.5**	60	72.2	54.6	93.5	84.3	125.4	134.6
Locking Range	**8.6GHz (10.9%)****	1.8GHz (3.1%)**	6.3GHz (9.12%)* 3.8GHz (5.5%)**	5.8GHz (11.2%)* 2GHz (3.8%)**	2.1GHz (2.3%)**	11.2GHz (14.2%)**	3GHz (2.4%)**	0.4GHz (0.29%)**
Pin [dBm]	**0**	0	7	2	0	3	-6	-8.5
P_{DC} [mW]	**7.88**	13	2	3	3.7	10.8	9.1	2.3
FoM1 [GHz^2/mW^2]	**90.04**	8.3	27.37	22.97	53.07	43.81	164.6	165.7
FoM2 [%/mW^2]	**4.19**	0.7	1.62	2.4	1.84	1.98	3.18	2.7
Phase noise @ 1MHz offset	**-117.13dBc/Hz**	-131.36dBc/Hz	-120.85dBc/Hz	-115dBc/Hz	-124.1dBc/Hz	-125.43dBc/Hz	N/A	> -115dBc/Hz
Area [mm^2]	**0.22*****	0.68	0.069***	0.09***	0.56	0.52	0.04***	0.46

$$FoM_1 = \frac{LR(GHz) \times f_{max}(GHz)}{P_{in}(mW) \times P_{DC}(\mathrm{mW})} \qquad FoM_2 = \frac{LR(GHz)}{f_{center}(\mathrm{GHz})} \times 100\% \times \frac{Division\ ratio}{P_{in}(mW) \times P_{DC}(\mathrm{mW})}$$

[1] H. Wu and L. Zhang, "A 16-to-18 GHz 0.18 μm Epi-CMOS divide-by-3 injection locked frequency divider," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2006, pp. 602–603.

[2] T.-N. Luo *et al.*, "A 60-GHz 0.13-μm CMOS divide-by-three frequency divider," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 11, pp. 2409–2415, Nov. 2008.

[3] C.-H. Wang *et al.*, "A 66-72 GHz divide-by-3 injection locked frequency divider in 0.13- m CMOS technology," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 344–347.

[4] X. P. Yu *et al.*, "A 3 mW 54.6 GHz divide-by-3 injection locked frequency divider with resistive harmonic enhancement," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 9, pp. 575–577, Sep. 2009.

[5] Y.-L. Yeh and H.-Y. Chang, "Design and analysis of a -band divide-by-3 injection locked frequency divider using second harmonic enhancement technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1617–1625, Jun. 2012.

[6] Y.-W. Chen *et al.*, "A W-Band harmonically enhanced CMOS divide-by-three frequency divider," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 4, pp. 257–259, Apr. 2014.

[7] I.-T. Lee *et al.*, "D-band divide-by-3 injection-locked frequency divider in 65 nm CMOS," *Electron. Lett.*, vol. 48, no. 17, pp. 1041-1042, Aug. 2012.

Acknowledgements

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